



SERVICE MANUAL

PMR446 FM TRANSCEIVER

IC-F25SR

S-14328XZ-C1
Feb. 2007

Icom Inc.

INTRODUCTION

This service manual describes the latest service information for the **IC-F25SR** PMR446 FM TRANSCEIVER at the time of publication.

MODEL	VERSION
IC-F25SR	[EUR-17]
	[UK-17]
	[EUR-18]
	[UK-18]

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

CAUTION

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 8 V. This will ruin the transceiver.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1110003491 S.IC TA31136FNG IC-F25SR MAIN UNIT 5 pieces
8820001210 Screw 2438 screw IC-F25SR Top cover 10 pieces
Addresses are provided on the inside back cover for your convenience.



REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 50 dB to 60 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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SECTION 1

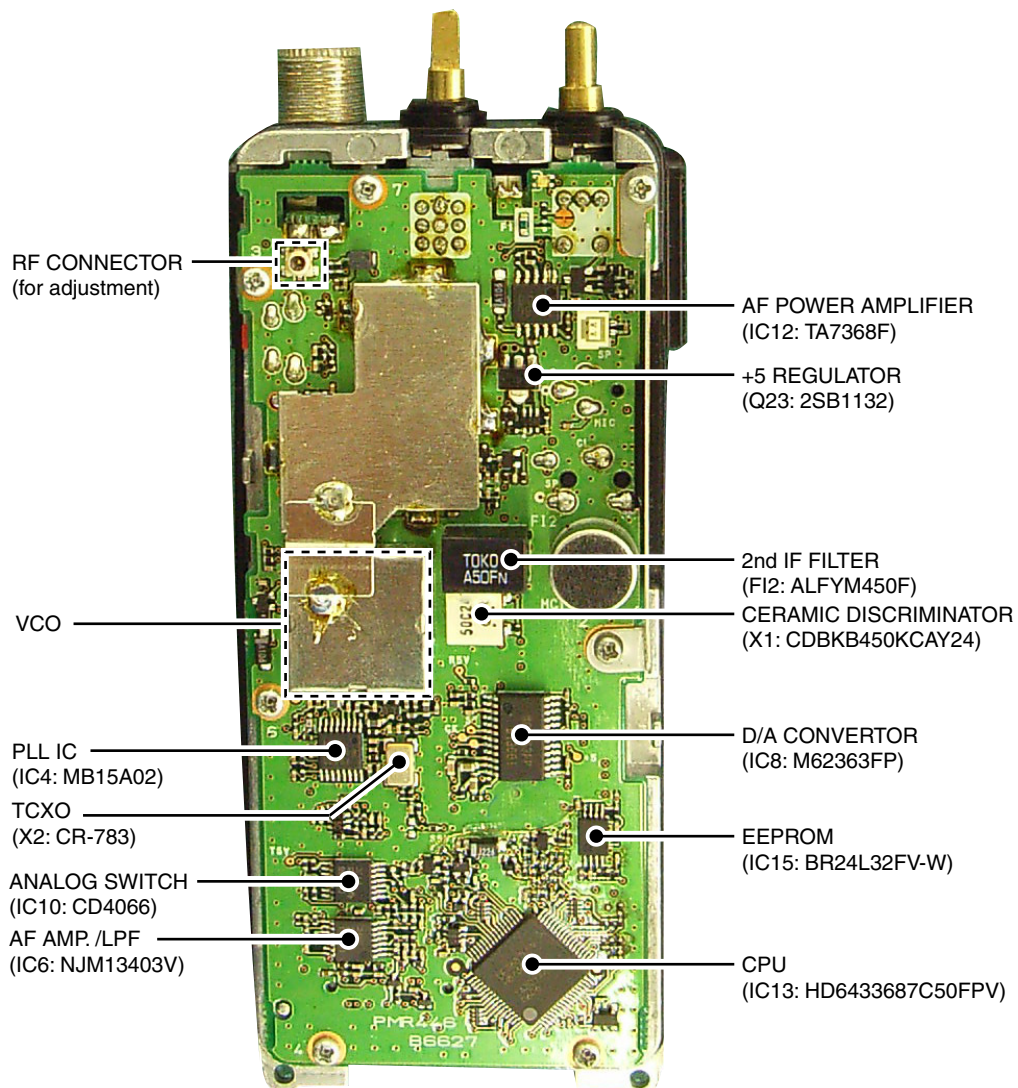
SPECIFICATIONS

GENERAL	• Frequency coverage		446.00625–446.09375 MHz	
	• Type of emission		8K50F3E (12.5 kHz)	
	• Number of programable channels		15 channels	
	• Antenna impedance		50 Ω (nominal)	
	• Operating temperature range		–25°C to 55°C	
	• Power supply		Specified Icom's battery packs only (Operatable voltage; 7.2 V DC negative ground)	
	• Current drain (approx.)	RX	Stand-by	75 mA
			Max. audio	300 mA
		TX	0.4 A (0.5 W EPR)	
	• Dimensions (projections included)		53.0 (W) × 195.0 (H) × 38.0 (D) mm	
• Weight (with antenna and BP-231, approx.)		260 g		
TRANSMITTER	• Transmit output power		0.5 W ERP	
	• Modulation		Variable reactance frequency modulation	
	• Max. permissible deviation		±2.5 kHz	
	• Frequency error		±0.5 kHz	
	• Spurious emission		0.25 μW (≤1 GHz), 1.00 μW (>1 GHz)	
	• Adjacent channel power		60 dB	
	• Audio harmonic distortion		5% typ. (with 1 kHz at AF 60% deviation)	
	• Residual modulation		50 dB typ.	
	• Limiting charact of modulation		70–100% of max. deviation	
	• Microphone impedance		2.2 kΩ	
	RECEIVER	• Receive system		Double conversion superheterodyne
• Intermediate frequencies		1st IF; 46.35 MHz, 2nd IF; 450 kHz		
• Sensitivity		26.5 dBμV/m at 20 dB SINAD		
• Squelch sensitivity (at threshold)		26.5 dBμV/m		
• Adjacent channel selectivity		81.29 dBμV/m		
• Spurious response		91.29 dBμV/m		
• Intermodulation		86.29 dBμV/m		
• FM Hum and Noise		50 dB typ.		
• Audio output power		0.5 W typ. at 5% distortion with an 8 Ω load 0.6 W typ. at 5% distortion with a 6 Ω load		
• Audio output impedance		8 Ω		

Measurements made in accordance with EN 300 296.

All stated specifications are subject to change without notice or obligation.

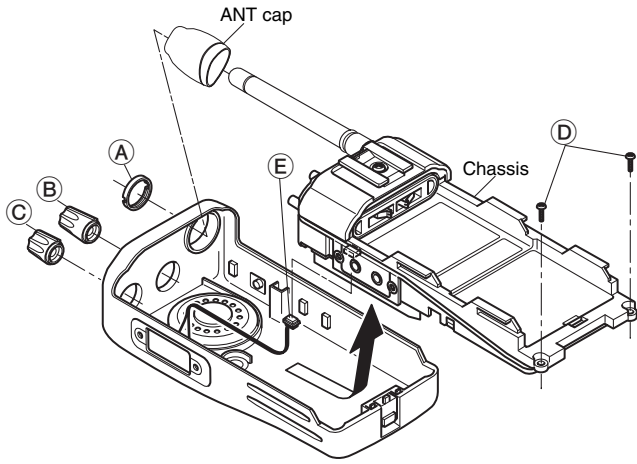
• MAIN UNIT



SECTION 3 DISASSEMBLY INSTRUCTION

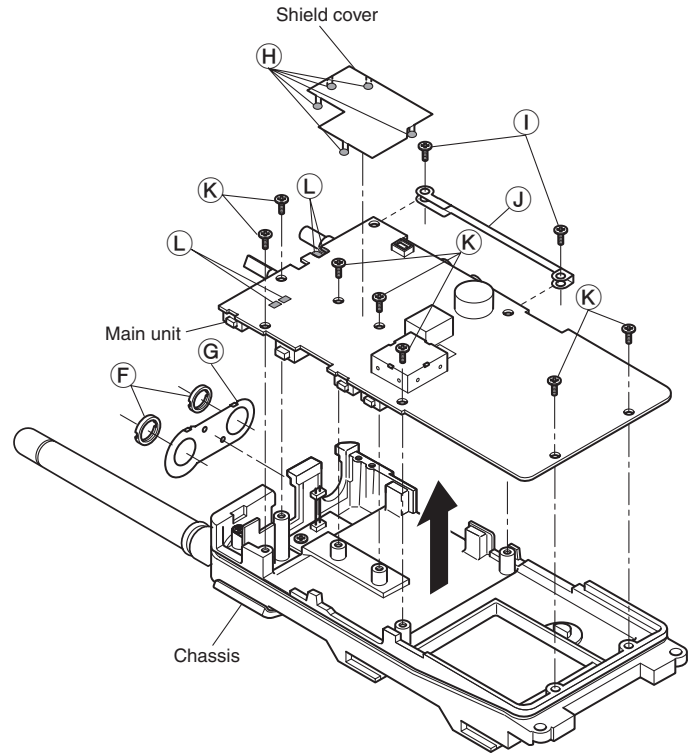
1. Removing the the CAHSSIS

- ① Remove ANT cap, and unscrew 1 nut (A) and 2 knobs (B), (C).
- ② Unscrew 2 screws (D).
- ③ Unplug the SP connector (E) from the MAIN UNIT.
- ④ Take off the chassis in the direction of the arrow.



2. Removing the MAIN UNIT

- ① Unscrew 2 nuts (F), and remove the top plate (G).
- ② Unsolder 5 points (H), and remove the shield cover.
- ③ Unscrew 2 screws (I), and remove the side plate (J).
- ④ Unscrew 7 screws (K).
- ⑤ Unsolder 4 points (L), and take off the main unit in the direction of the arrow.



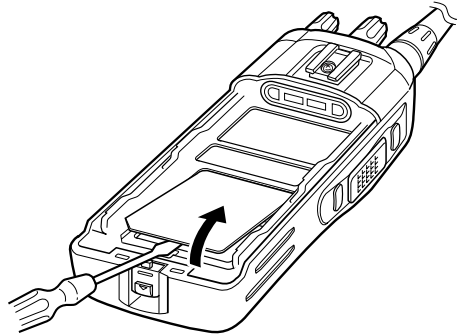
SECTION 4 OPTIONAL UNITS INSTALLATION

Install optional unit as follows:

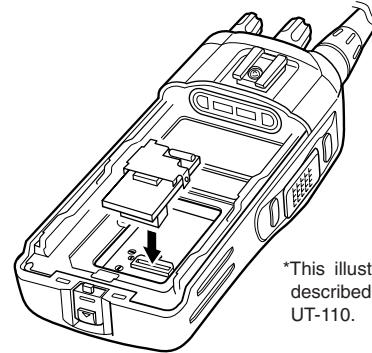
① Rotate [VOL] to turn the power OFF, and remove the battery pack.

② Remove the unit cover.

NOTE: Use a flat head screw driver or a similar flat instrument, and insert into the hollow of the chassis, then lift and take away the unit cover. (The removed cover cannot be used gain.)



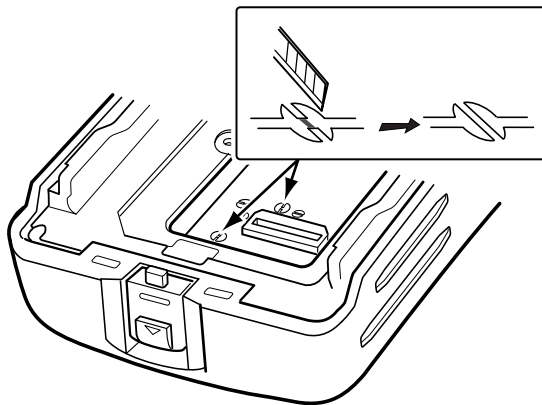
④ Install the unit as shown below.



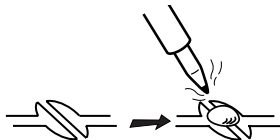
*This illustration is described with the UT-110.

⑤ Replace the unit cover and the battery pack, then rotate [VOL] to turn the power ON.

③ Cut the pattern on the PCB at the TX mic circuit (MIC) and RX AF circuit (DISC) as shown below.



NOTE: When uninstalling the scrambler unit. Be sure to re-solder the disconnected points at left, otherwise no TX modulation or AF output is available.



5-1 RECEIVER CIRCUITS

5-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit toggles the receive (RX) line and transmit (TX) line.

The received signals from the antenna are passed through the low-pass filter (LPF; L709, L710, C742, C744–C748) and antenna switch (D2, D5).

While transmitting, the voltage on the T5V line is applied to D2 and D5, and these are ON. Thus the TX line is connected to the antenna. Simultaneously, the RX line is connected to the GND to prevent transmit signal entering.

While receiving, no voltage is applied to the D2 and D5, and these are OFF. Thus the TX line and the antenna is disconnected to prevent received signals entering. Simultaneously, the RX line is disconnected from the GND and the received signals are passed through the LPF (L712, C750–C752). The filtered signals are applied to the RF circuits.

5-1-2 RF CIRCUITS

RF circuits filter and amplify the received signals within the frequency coverage.

The received signals from the antenna switching circuit are passed through the two-staged bandpass filter (BPF; D19, D25, L7, L8, C21–C23, C25, C27–C29) to filter-out unwanted signals, and the filtered signals are applied to the RF amplifier (Q2). The amplified received signals are then applied to the 1st mixer (Q3) via another two-staged BPF (D14, D15, L9, L11, C19, C36, C39–C41, C44, C45).

5-1-3 1st IF CIRCUITS

The received signals are converted into the 1st IF signal, filtered and amplified at the 1st IF circuits.

The received signals from the two-staged BPF (D14, D15, L9, L11, C19, C36, C39–C41, C44, C45) are applied to the 1st mixer (Q6) and converted into the 46.35 MHz 1st IF signal by being mixed with the local oscillator (LO) signal from the RX VCO (Q14, D16, D22).

The converted 1st IF signal is passed through the 1st IF filter (F1) to filter-out adjacent signals, then applied to the 1st IF amplifier (Q7). The amplified 1st IF signal is then applied to the IF IC (IC1, pin 16).

5-1-4 2nd IF AND DEMODULATOR CIRCUITS

The 1st IF signal is converted into the 2nd IF signal, and demodulated.

The 1st IF signal from the 1st IF amplifier is applied to the 2nd mixer in the IF IC (IC1, pin 16), and converted into the 450 kHz 2nd IF signal by being mixed with the 45.9 MHz 2nd LO signal from the reference frequency oscillator (X2) via the tripler (Q19) and BPF (L33, C163, C164, C166). The converted 2nd IF signal is output from pin 3, and passed through the 2nd IF filters to remove sideband noise.

The 2nd IF signal is passed through the 2nd IF filter (F12) and applied to the IF IC (IC1, pin 5) again via A/D switches (D2, D3).

The filtered 2nd IF signal is amplified at the limiter amplifier, and FM-demodulated by the quadrature detector (IC9, pins 10, 11, X1). The demodulated AF signals are output from pin 9, then applied to the AF amplifier circuits.

5-1-5 AF AMPLIFIER CIRCUITS

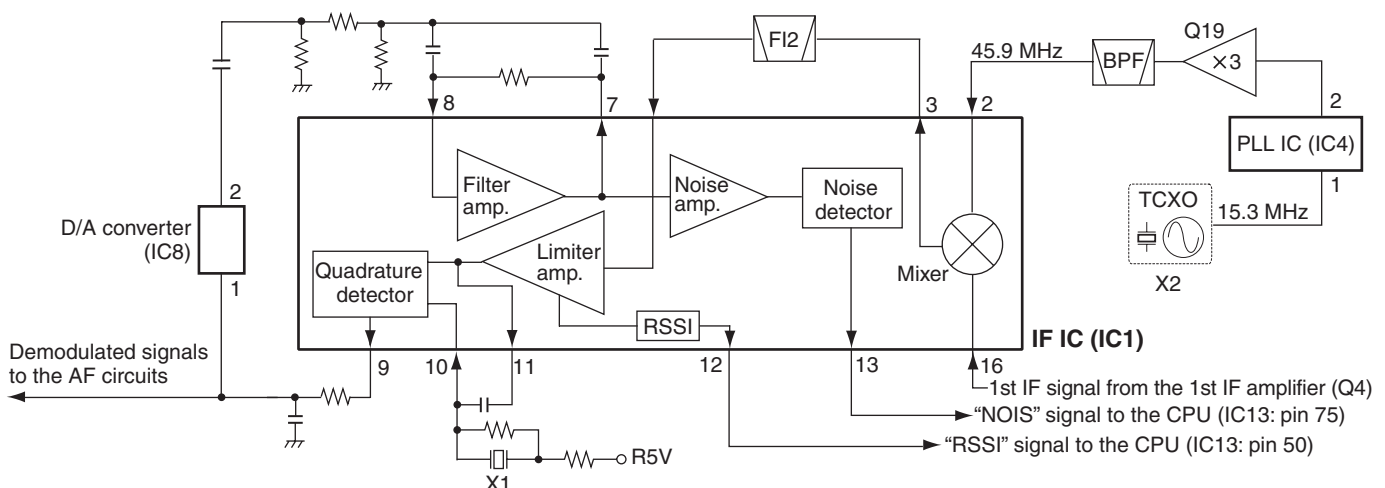
The demodulated AF signals from the IF IC are amplified and filtered at AF circuits.

The demodulated AF signals from the IF IC (pin 9) are passed through HPF (IC6, pins 1, 2) to remove tone signals. The filtered AF signals are passed through the de-emphasis circuit (R142, C249) to obtain the –6 dB/oct of frequency characteristic. The de-emphasized AF signals are passed through the RX mute switch (Q34), analog switch (IC10, pins 3, 4), LPF (IC6, pins 13, 14), analog switch (IC10, pins 1, 2), AF mixer (IC6, pins 6, 7) and analog switch (IC3, pins 10, 11) in sequence.

The AF signal from the analog switch (IC3, pin 11) are adjusted its level (=audio level) by volume control pot (R226), then applied to the AF power amplifier (IC12, pin 4) and amplified to the 0.5 W of audio output power (max., at 8 Ω load).

The power-amplified AF signals are output from pin 10, then applied to the speaker (CHASSIS UNIT; SP1) or an external speaker via [SP] jack (J2).

• 2nd IF AND DEMODULATOR CIRCUITS



5-1-6 SQUELCH CIRCUITS

5-1-6-1 NOISE SQUELCH

The squelch mutes the AF output signals when no RF signals are received. By detecting noise components (around 30 kHz signals) in the demodulated AF signals, the squelch circuit toggles the mute switch and AF power amplifier ON and OFF.

A portion of the demodulated AF signals from the IF IC (IC1, pin 9) are applied to the D/A converter (IC8, pin 24) for level (=squelch threshold) adjustment. The level-adjusted AF signals are output from pin 23 and passed through the noise filter (IC1, pins 7, 8, R42, R44–R46, C69, C70, C413). The filtered noise signals are amplified the noise components only at the noise amplifier.

The amplified noise components are converted into the pulse-type signal at the noise detector section, and output from pin 13 as the "NOIS" signal. The converted signal is applied to the CPU (IC13, pin 75). Then the "RMUTE" signal from the CPU (IC13, pin 96) to the RX mute switch (Q34) and analog switch (IC3, pins 12, 13) becomes "Low" according to the "NOIS" signal level to cut off the AF line.

At the same time, the "AFON" signal from the CPU (IC13, pin 70) to the AF amplifier controller (Q30, Q31) becomes "Low", and the controller turns the AF power amplifier (IC12) OFF.

5-1-6-2 TONE SQUELCH

• CTCSS/DTCS

The tone squelch circuit detects tone signals and opens the squelch only when receiving a signal containing a matched sub audible tone. When the tone squelch is in use, and a signal with a mismatched or no sub audible tone is received, the tone squelch circuit mutes the AF signals even when the noise squelch is open.

A portion of the demodulated AF signals are passed through the active LPF (Q39) to filters CTCSS/DTCS signal. The filtered signal is applied to the CPU (IC13, pin 46). The CPU compares the applied signal and the set CTCSS/DTCS, then the CPU controls the status ("Low" or "High") of "RMUTE" and "AFON" signals as same as "NOISE SQUELCH."

• DTMF

DTMF signals in the demodulated AF signals are passed through the LPF (Q36) to remove unwanted components (voice signals), then applied to the CPU (IC13, pin 45) and decoded.

5-2 TRANSMITTER CIRCUITS

5-2-1 MICROPHONE AMPLIFIER CIRCUITS

The AF signals from the microphone (MIC signals) are filtered and level-adjusted at microphone amplifier circuits.

• MIC SIGNALS

MIC signals from the microphone are applied to or bypassed the ALC (Automatic Level Control) circuit (IC24, pins 3, 5) and the A/D switch (IC25, pins 1, 7), then applied to the D/A converter (IC8, pin 1).

The level-adjusted MIC signals are output from pin 2, and passed through the MIC mute switch (Q35), HPF (IC6, pins 13, 14) and gain switch (Q34, Q35) which controls the gain of MIC amplifier (IC5) according to the Analog/Digital mode, then applied to the MIC amplifier (IC5, pin 9). The amplified MIC signals are output from pin 8, and passed through the analog switch (IC3, pins 3, 4), AF mixer (IC5, pins 6, 7) where the MIC signals and tone signals are mixed with.

• TONE SIGNALS

The CTCSS/DTCS signals are generated by the CPU (IC13) and output from pins 19–21. The output signals are passed through the 3 registers (R222–R224) to change its wave form. The wave form changed CTCSS/DTCS signals are passed through the LPF (IC7, pins 8, 10), tone filter switch (Q40) and D/A converter (IC8, pins 11, 12) for level adjustment. The level adjusted CTCSS/DTCS signals are then applied to the AF mixer (IC5, pin 6).

DTMF signals are generated by the CPU (IC13) and output from pin 43. The output DTMF signals are passed through two LPF's (IC6, pins 1, 3 and pins 12, 14), then applied to the AF mixer (IC5, pin 6).

The mixed AF signals are output from pin 7 of the AF mixer (IC5) and passed through the analog switch (IC3, pins 8, 9), then applied to another AF amplifier (IC7, pin 6). The amplified AF signals are output from pin 7, and applied to the D/A converter (IC8, pin 9) to be adjusted its level (=deviation). The level-adjusted MIC signals are then applied to the modulation circuits as the modulation signals.

5-2-2 MODULATION CIRCUITS

The modulation circuits modulates the VCO oscillating signal using the modulation signals.

The modulation signals from the D/A converter (IC8, pin 10) are applied to the D18 at the TX VCO (Q13, D17, D18, D21) to modulate the VCO oscillating signal by changing the reactance of D18.

The modulation signals are also applied to the reference frequency oscillator (X2) via D/A converter (IC8, pins 15, 16) to ensure the modulation of low frequency components of the modulation signals.

The modulated VCO output is buffer-amplified by Q12 and Q10, then applied to the transmit amplifiers as the transmit signal via TX/RX switch (D14=ON, D15=OFF).

5-2-3 TRANSMIT AMPLIFIERS

The transmit signal from the VCO is amplified to the transmit output level by the transmit amplifiers.

The transmit signal from the TX/RX switch (D14=ON, D15=OFF) is amplified by two pre-drive amplifiers (Q5), drive amplifier (Q8) and power amplifier (Q7) in sequence to obtain 0.5 W (approx.) of transmit output power.

The power-amplified transmit signal is passed through the antenna switch (D2) and LPF (as a harmonic filter; L709, L710, C742, C744–C748), then applied to the antenna via the ANT UNIT.

5-2-4 APC CIRCUIT

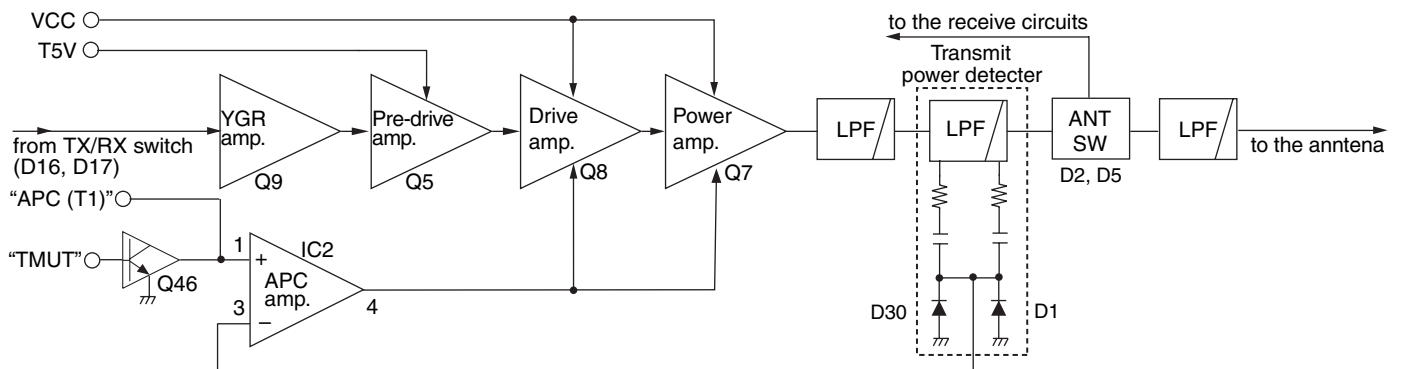
The APC (Automatic Power Control) circuit prevents the transition of the transmit output power level which is caused by load mismatching or heat effect, etc.

A portion of transmit signal is detected by the transmit power detector (D1, D30) to produce a DC voltage corresponding to the transmit output power level. The detected voltage is applied to the APC amplifier (IC2, pin 3). The transmit power setting voltage “APC (T1)” from the D/A converter (MAIN UNIT; IC8, pin 1) is applied to another input terminal (pin 1) as the reference voltage.

The APC amplifier compares the detected voltage and reference voltage, and the difference of the voltage “APCV” is output from pin 4. The voltage “APCV” controls the bias of the drive (Q8) and power (Q7) amplifiers to reduce/increase the gain of these amplifiers for stable transmit output power.

The transmit power muting is carried out by the TX mute switch (Q46), using the “TMUT” signal from the CPU (IC13, pin 35).

• APC CIRCUIT



5-3 PLL CIRCUITS

5-3-1 VCO

VCO is a oscillator whose oscillating frequency is controlled by adding voltage (lock voltage).

This transceiver has 2 VCO's; RX VCO (Q14, D16, D22) and TX VCO (Q13, D17, D18, D21). The RX VCO oscillates the 1st LO signals, and the TX VCO oscillates the transmit signal.

• RX VCO

The output signals are amplified by the buffer amplifiers (Q15, Q29), and applied to the 1st mixer (Q3) via TX/RX switch (D14 is OFF, D15 is ON) and LPF (L12, L46, C46, C47, C396, C397), to be mixed with the received signals to produce the 46.35 MHz 1st IF signal.

• TX VCO

The output signal is applied to the transmit amplifiers via the buffer amplifiers (Q10, Q12) and TX/RX switch (D14 is ON, D15 is OFF).

A portion of each VCO output is applied to the PLL IC (IC4, pin 8) via the buffer amplifier (Q11) and the LPF (L32, L34, C196, C197, C205).

5-3-2 PLL IC

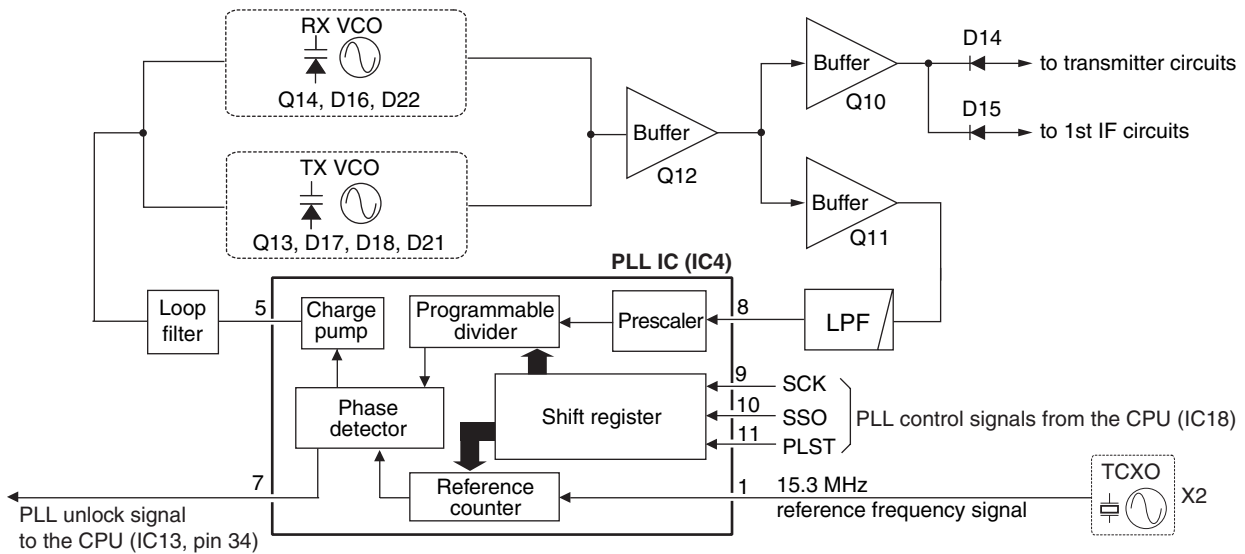
The PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output frequency is controlled by the divided ratio (N-data) from the CPU.

The VCO output signals from the BPF (L32, L34, C196, C197, C205) are applied to the PLL IC (IC4, pin 8). The applied signals are divided at the prescaler and programmable counter according to the "SSO" signal from the CPU (IC13, pin 99). The divided signal is phase-compared with the reference frequency signal from the reference frequency oscillator (X2), at the phase detector.

The phase difference is output from pin 5 as a pulse type signal after being passed through the internal charge pump. The output signal is converted into the DC voltage (lock voltage) by passing through the loop filter (R94-R96, C16, C17, C146). The lock voltage is applied to the varactors (D9 and D11 of RX VCO, D10 and D13 of TX VCO) and locked to keep the VCO frequency constant.

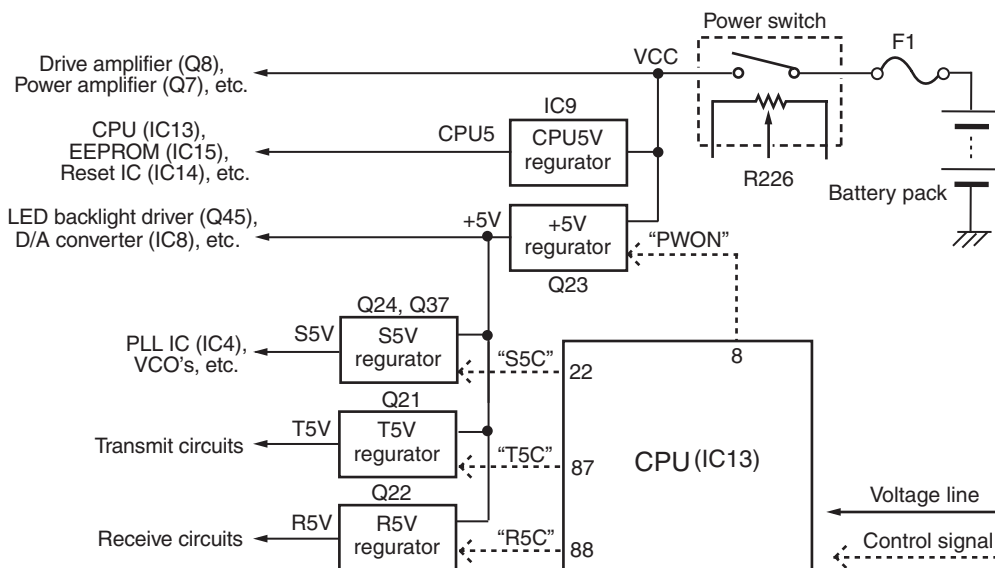
If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the VCO oscillating frequency.

• PLL CIRCUIT



5-4 POWER SUPPLY CIRCUITS

Voltage from the attached battery pack is routed to whole of the circuit in the transceiver via a switch and regulators.



5-5 PORT ALLOCATIONS

5-5-1 CPU (IC13)

Pin No.	Port Name	Description
1-3	KR1-KR3	Input ports for dealer-programmable keys.
4-8	KS0-KS4	Output ports for dealer-programmable keys.
9	BUSY	Outputs "BUSY" signal to the DSP UNIT.
10	CCS	Outputs chip-select signal to the DSP UNIT.
11	SCK	Outputs serial clock signal to the PLL IC (IC4, pin 9) and D/A converter (IC8, pin 7/IC23, pin 7).
19-21	CENC0-CENC2	Output ports for CTCSS/DTCS signal.
22	S5C	Outputs S5V line control signal to the S5V regulator (Q23). "Low"=While power save mode.
26	T5C	Outputs T5V line control signal to the T5V line regulator (Q24, Q49). "Low"=While transmitting.
27	R5C	Outputs R5V line control signal to the R5V line regulator (Q25). "Low"=While receiving.
31	PLST	Outputs PLL strobe signal to the PLL IC (IC4, pin 11).
34	ULCK	Input port for PLL unlock detect signal from the PLL IC (IC4, pin 7). "Low"=While the PLL circuit is unlocked.
35	TMUT	Outputs transmit mute signal to the transmit mute switch (Q46). "High"=Transmitting is muted.
36	MONI	Input port for [SIDE1] key (S5). "Low"=While the key is pushed.
37	EMER	Input port for top switch (S1). "Low"=While the switch is pushed.
39	DSDA	Outputs serial data to the D/A converter (IC23, pin 6).
43	SENC	Outputs DTMF signals to the LPF (IC6, pin 3).
44	BEEP	Outputs beep sounds to the D/A converter (IC8, pin 21).
45	SDEC	Input port for DTMF signals.
46	CDEC	Input port for CTCSS/DTCS signals.
48	BATV	Input port for remaining battery power.
49	LVIN	Input port for VCO lock voltage.
50	RSSI	Input port for receive signal strength level signal from the IF IC (IC1, pin 12).
59	RES	Input port for CPU reset signal from the reset IC (IC14, pin 1). "Low"=When the CPU is reset.
69	CSFT	Outputs CPU clock shift signal to the clock shift switch (D6).
70	AFON	Outputs AF power amplifier (IC12) control signal to the AF power amplifier controller (Q41, Q42, D21, D23). "High"=The AF power amplifier is ON.
71	DAST	Outputs strobe signal to the D/A converter (IC8, pin 6).
72	DUSE	Outputs CTCSS/DTCS select signal to the tone filter switch (Q40). "High"=While DTCS is in use.
75	NOIS	Input port for noise signal from the IF IC (IC1, pin 13).
82	ESDA	Outputs serial data to the EEPROM (IC15, pin 5).
85	ESCL	Outputs clock signal to the EEPROM (IC15, pin 6).

Pin No.	Port Name	Description
89	DIGI	Outputs Analog/Digital select signal to the A/D switch (D2, D3). "High"=Digital mode is selected.
96	RMUTE	Outputs AF mute signal to the analog switch (IC3, pins 12, 13). "Low"=While the squelch is close or transmitting.
97	MMUTE	Outputs MIC signals mute signal to the analog switch (IC3, pin 5) and MIC mute switch (Q31). "Low"=While receiving.
99	SSO	Outputs serial data to the PLL IC (IC4, 10) and D/A converter (IC8, pin 8).
100	KR0	Input ports for dealer-programmable keys.

5-5-2 D/A CONVERTER (IC6)

Pin No.	Port Name	Description
2	SQLIN	Outputs level-adjusted AF signals to the noise filter (IC9, pins 7, 8, R42, R44-R46, C69, C70, C413).
3	MOD	Outputs modulation signals to the TX VCO (Q13, 17, D18, D21)
4	RXLVA	Outputs oscillating frequency adjust voltage to the TX and RX VCO.
10	BEEPO	Outputs beep sounds to the AF volume buffer (IC6, pin 9).
11	BAL	Outputs modulation balance control signal to the reference frequency oscillator buffer (IC7, pin 12).
14	LVA	Outputs oscillating frequency adjust voltage to the TX and RX VCO.
15	REF	Outputs reference frequency control voltage to the reference frequency oscillator (X2).
22	T1	<ul style="list-style-type: none"> • While receiving Outputs BPF tuning voltage to the tunable BPF (D19, D25, L7, L8, C21-C23, C25, C27-C29). • While transmitting (as "APC" signal) Outputs transmit mute signal to the transmit mute switch (Q46).
23	T2	Outputs BPF tuning voltage to the tunable BPF (D14, D15, L9, L11, C19, C36, C39-C41, C44, C45).

SECTION 6 ADJUSTMENT PROCEDURE

6-1 PREPARATION

When adjusting IC-F25SR, CS-F25SR CLONING SOFTWARE, CS-F25SR ADJ ADJUSTMENT SOFTWARE (Rev. 1.0 or later), OPC-478/U/UC JIG CABLE (modified OPC-478/U/UC CLONING CABLE; see the page 6-2) and the following test equipments are required.

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.2 V DC Current capacity : More than 1 A	External speaker	Input impedance : 8 Ω Capacity : 1 W or more
modulation analyzer	Frequency range : DC–600 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 20 or 30 dB Capacity : 1 W
Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 0.1–600 MHz Output level : 0.1 μV to 32 mV (–127 to –17 dBm)
RF power meter	Measuring range : 0.1–1 W Frequency range : 100–600 MHz Impedance : 50 Ω SWR : Better than 1.2 : 1	Oscilloscope	Frequency rang : DC–20 MHz Measuring range : 0.01–20 V

■ SYSTEM REQUIREMENTS (for the ADJUSTMENT SOFTWARE)

- Microsoft® Windows® 98/98SE/Me/2000/XP
- RS-232C serial port (D-sub 9 pin) or USB port

■ ADJUSTMENT SOFTWARE INSTALLATION

- ① Quit all applications when Windows is running.
- ② Insert the CD into the appropriate CD drive.
- ③ Double-click the “Setup.exe” contained in the ‘CS-F25SR ADJ’ folder in the CD drive.
- ④ The “Welcome to the InstallShield Wizard for CS-F25SR ADJ” will appear. Click [Next>].
- ⑤ The “Choose Destination Location” will appear. Then click [Next>] to install the software to the destination folder. (e.g. C:\Program Files\icom\CS-F25SR ADJ)
- ⑥ After the installation is completed, the “InstallShield Wizard Complete” will appear. Then click [Finish].
- ⑦ Eject the CD.
- ⑧ Program group ‘CS-F25SR ADJ’ appears in the ‘Programs’ folder of the start menu, and ‘CS-F25SR ADJ’ icon appears on the desk top screen.

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■ BEFORE STARTING SOFTWARE ADJUSTMENT

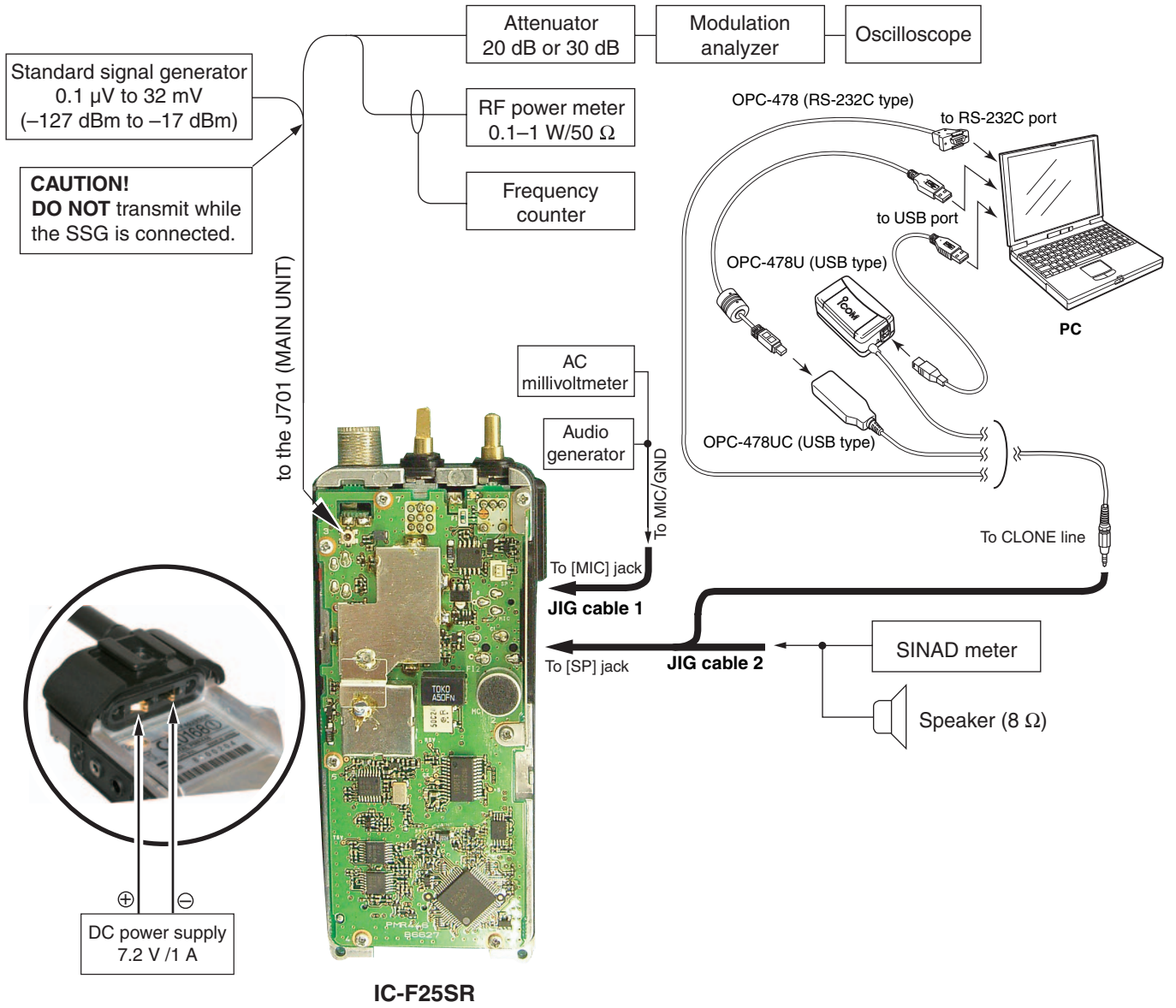
Clone the adjustment frequencies and settings into the transceiver, and set the configuration using the CS-F25SR CLONING SOFTWARE before starting the software adjustment. Otherwise, the software adjustment can not be started.

CAUTION!: **BACK UP** the originally programmed memory data in the transceiver before programming the adjustment frequencies. When program the adjustment frequencies into the transceiver, the transceiver’s memory data will be overwritten and lose original memory data at the same time.

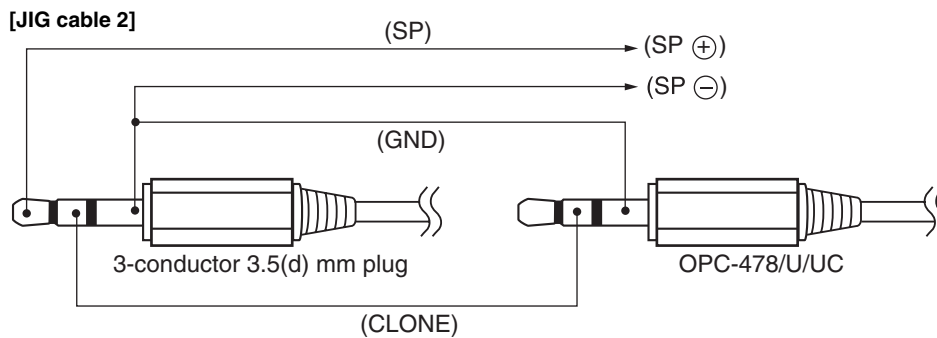
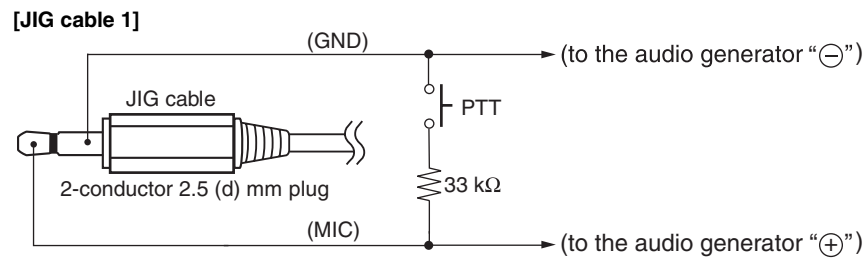
• ADJUSTMENT FREQUENCY LIST

CHANNEL	FREQUENCY	SETTING
1-1	446.006250 MHz	None
1-2	446.006250 MHz	• DTCS code : 071
1-3	446.006250 MHz	• CTCSS frequency : 151.4 Hz

• CONNECTION



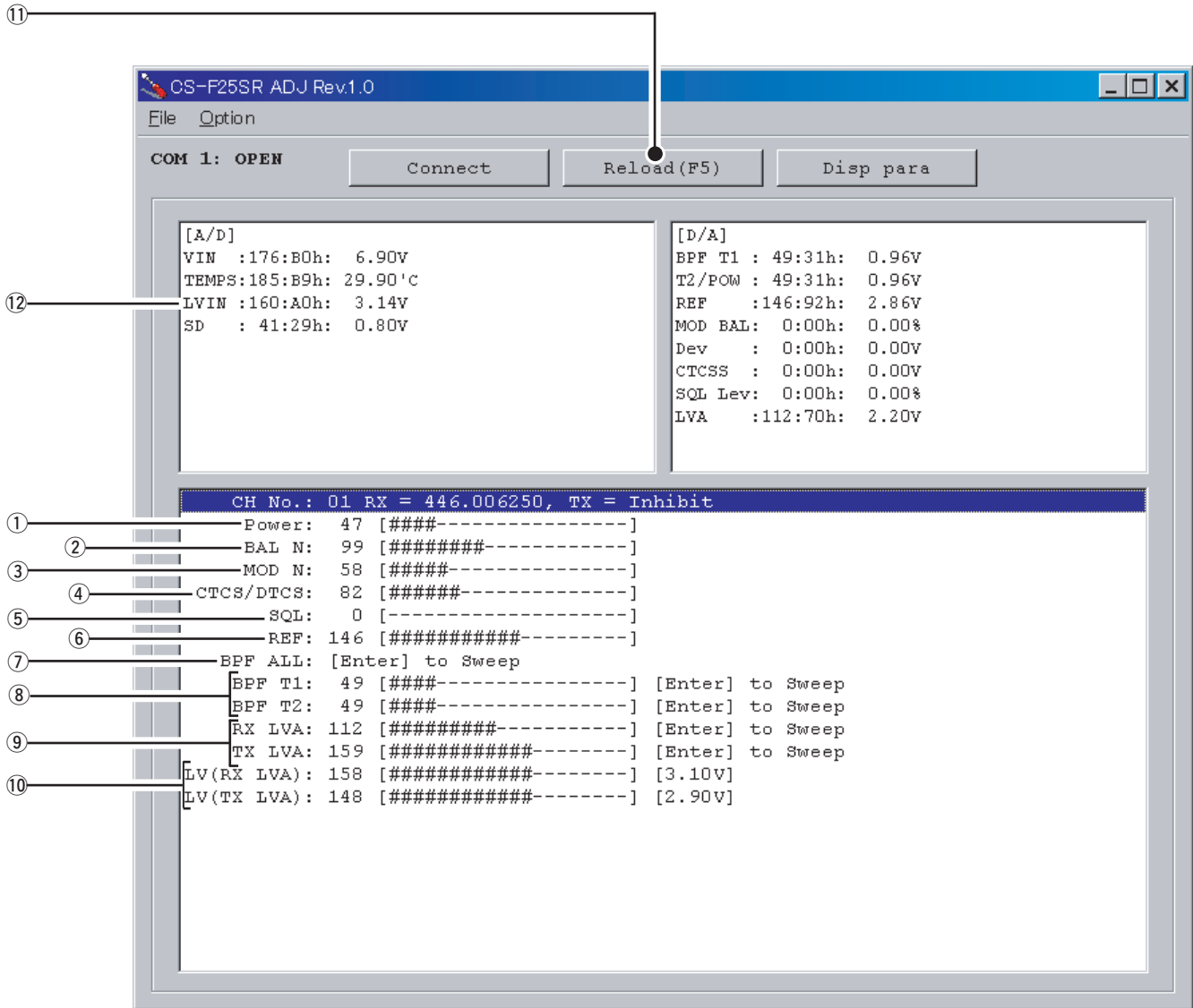
• JIG CABLES



■ STARTING SOFTWARE ADJUSTMENT

- ① Connect the transceiver and PC with OPC-478/U/UC JIG CABLE.
- ② Turn the transceiver power ON.
- ③ Boot up Windows, and click the program group 'CS-F25SR ADJ' in the 'Programs' folder of the [Start] menu, then CS-F25SR ADJ's window appears.
- ④ Click 'Connect' on the CS-F25SR ADJ's window, then the window shows transceiver's condition and adjustment items as below.
- ⑤ Set or modify adjustment data as specified.

• PC SCREEN EXSAMPLE



NOTE: The above values for settings are example only.
 Each transceiver has its own specific values for each setting.

- | | |
|-------------------------|---------------------------------------|
| ① Transmit output power | ⑦ Receive sensitivity (Automatically) |
| ② Modulation balance | ⑧ Receive sensitivity (Manually) |
| ③ FM deviation | ⑨ PLL lock voltage |
| ④ CTCSS/DTCSS deviation | ⑩ PLL lock voltage preset |
| ⑤ Squelch | ⑪ Reload data |
| ⑥ Reference frequency | ⑫ PLL lock voltage (verify) |

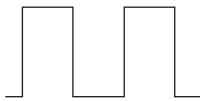
6-2 FREQUENCY ADJUSTMENT

Select an adjustment item using [↑] / [↓] keys, then set to the specified value using [←] / [→] keys on the connected PC's keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	OPERATION	
PLL LOCK VOLTAGE [RX LVA]	1 <ul style="list-style-type: none"> • Channel : 1-1 • Lock voltage preset [LV (RX LVA)] : 158 [3.1 V] • Receiving 	PC screen	Click [Reload (F5)] button, then check the "LVIN" item on the ADJ's screen (see page 6-3).	Push [Enter] key (Automatic adjustment)
[TX LVA]	3 <ul style="list-style-type: none"> • Channel : 1-1 • Lock voltage preset [LV (TX LVA)] : 148 [2.9 V] • Connect an RF power meter to the RF connector (MAIN UNIT; J701). • Transmitting 			
REFERENCE FREQUENCY [REF]	<ul style="list-style-type: none"> • Channel : 1-1 • Connect an RF power meter to the RF connector (MAIN UNIT; J701). • Transmitting 	MAIN UNIT	Loosely couple a frequency counter to the RF connector (MAIN UNIT; J701).	446.006250 MHz

6-3 TRANSMIT ADJUSTMENT

Select an adjustment item using [↑] / [↓] keys, then set to the specified value using [←] / [→] keys on the connected PC's keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	OPERATION	
TRANSMIT OUTPUT POWER [Power]	1 <ul style="list-style-type: none"> • Channel : 1-1 • Transmitting 	MAIN UNIT	Connect an RF power meter to the RF connector (MAIN UNIT; J701).	0.5 W
FM DEVIATION [MOD N]	1 <ul style="list-style-type: none"> • Channel : 1-1 • Connect the modulation analyzer to the RF connector (MAIN UNIT; J701) through an attenuator, and set as; <ul style="list-style-type: none"> HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • Connect an audio generator to the [MIC] jack through the JIG cable and set as; <ul style="list-style-type: none"> Frequency : 1.0 kHz Level : 150 mV rms • Transmitting 	MAIN UNIT	Connect the modulation analyzer to the RF connector (MAIN UNIT; J701) through an attenuator.	±2.05 to ±2.15 kHz
MODULATION BALANCE [BAL N]	1 <ul style="list-style-type: none"> • Channel : 1-2 • No audio signals applied to the JIG cable. • Set the modulation analyzer to the same condition as "FM DEVIATION." • Transmitting 	MAIN UNIT	Connect the modulation analyzer with the oscilloscope to the RF connector (MAIN UNIT; J701) through an attenuator.	Set to square wave form 
CTCSS/DTCS DEVIATION [CTCS/DTCS]	1 <ul style="list-style-type: none"> • Channel : 1-3 • No audio signals applied to the JIG cable. • Set the modulation analyzer to the same condition as "FM DEVIATION." • Transmitting 	MAIN UNIT	Connect the modulation analyzer to RF connector (MAIN UNIT; J701) through an attenuator.	±0.33 to ±0.37 kHz

6-4 RECEIVE ADJUSTMENT

Select an adjustment item using [↑] / [↓] keys, then set to the specified value using [←] / [→] keys on the connected PC's keyboard.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE
		UNIT	LOCATION	
RECEIVE SENSITIVITY [BPF (T1)] [BPF (T2)]	1 <ul style="list-style-type: none"> • Channel : 1-1 • Connect an SSG to RF connector (MAIN UNIT; J701) and set as; <ul style="list-style-type: none"> Frequency : 446.006250 MHz Level : +20 dBμ[†] (-87 dBm) Modulation : 1 kHz Deviation : ±1.75 kHz • Receiving 	[MIC/SP] jack	Connect the SINAD meter with an 8 Ω load to the JIG cable.	Minimum distortion level
CONVENIENT: The "RECEIVE SENSITIVITY" can be adjusted automatically. 1: Put the cursor on "[BPF ALL]," then push [Enter] key. 2: The connected PC tunes BPF's to peak levels automatically.				
SQUELCH [SQL]	1 <ul style="list-style-type: none"> • Channel : 1-1 • Close the squelch by adjusting the value of [SQL] item on the CS-F25SR ADJ's screen. • Connect the SSG to RF connector (MAIN UNIT; J701) and set as; <ul style="list-style-type: none"> Frequency : 466.006250 MHz Level : -14 dBμ[†] (-121 dBm) Modulation : 1 kHz Deviation : ±1.75 kHz • Receiving 	[MIC/SP] jack	Connect an 8 Ω speaker to the JIG cable.	Set the [SQL] to the value that the audio signals just appears.

[†]: The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C307	4030017460	S.CER ECJ0EB1E102K	B	59.3/12.3
C308	4030017460	S.CER ECJ0EB1E102K	T	75.7/9.8
C309	4030017460	S.CER ECJ0EB1E102K	B	75.5/11.3
C310	4030016930	S.CER ECJ0EB1A104K	T	21.3/11.9
C311	4030017460	S.CER ECJ0EB1E102K	B	64.9/8.5
C312	4030017420	S.CER ECJ0EC1H470J	B	74.5/5.7
C313	4030017420	S.CER ECJ0EC1H470J	B	32.9/7.1
C314	4030017460	S.CER ECJ0EB1E102K	T	86.6/3.3
C315	4030017460	S.CER ECJ0EB1E102K	T	93.2/6
C316	4030016930	S.CER ECJ0EB1A104K	T	91.7/2.8
C317	4510008540	S.ELE EEE1CA100SR	B	95.9/15.2
C318	4030016930	S.CER ECJ0EB1A104K	T	89.7/8.9
C319	4030016930	S.CER ECJ0EB1A104K	T	89.6/2.8
C320	4030017730	S.CER ECJ0EB1E471K	T	88.6/2.8
C321	4030017460	S.CER ECJ0EB1E102K	B	19.3/4.2
C322	4030016950	S.CER ECJ0EB1A473K	T	93.9/13.9
C323	4030016950	S.CER ECJ0EB1A473K	T	87.6/9.7
C324	4030017420	S.CER ECJ0EC1H470J	T	85/13.7
C325	4550006250	S.TAN TEESVA 1A 106M8R	T	90.6/17.2
C326	4510008900	S.ELE EEEFC0J101P	B	87.8/8.9
C333	4030017420	S.CER ECJ0EC1H470J	B	76.8/39.9
C335	4030018860	S.CER ECJ0EB0J105K	B	57.2/21.1
C339	4030016930	S.CER ECJ0EB1A104K	B	5.9/17.2
C340	4030016930	S.CER ECJ0EB1A104K	B	9.3/12.5
C341	4030016930	S.CER ECJ0EB1A104K	B	5.9/10.1
C342	4030017630	S.CER ECJ0EC1H120J	B	18.3/4.2
C343	4030017580	S.CER ECJ0EC1H060C	B	5.6/4.2
C344	4030017640	S.CER ECJ0EC1H150J	B	7.6/9.1
C345	4030016930	S.CER ECJ0EB1A104K	B	11/11.2
C346	4030016930	S.CER ECJ0EB1A104K	B	11/10.1
C347	4030016790	S.CER ECJ0EB1C103K	T	8.8/6.5
C348	4030016930	S.CER ECJ0EB1A104K	T	6/10
C349	4030016930	S.CER ECJ0EB1A104K	T	21.3/14.9
C350	4030017460	S.CER ECJ0EB1E102K	T	59.4/43.4
C354	4030017460	S.CER ECJ0EB1E102K	T	14.2/24.4
C355	4030018080	S.CER ECJ0EB1H182K	T	43.9/22.7
C356	4030018910	S.CER C1608 JB 0J 475K-T	T	34.6/20.6
C357	4030017400	S.CER ECJ0EC1H220J	T	79/25.5
C358	4030017420	S.CER ECJ0EC1H470J	B	7.8/25.4
C359	4030017420	S.CER ECJ0EC1H470J	B	6.9/25.4
C360	4030017570	S.CER ECJ0EC1H040B	B	87.7/36.5
J1	6510021901	S.CNR BM02B-ASRS-TF (LF) (SN)	T	86.6/6.8
J2	6450001680	CNR HSJ1122-010010		
J3	6450002250	CNR HSJ1456-010320		
J4	6510018430	S.CNR AXN330C038P	B	11.8/30.6
J6	6510023350	S.CNR MM8430-2600RA1	T	93.9/39.3
F1	5210000830	S.FUS ERBF3R00U	T	98/14.5
DS1	5040002670	S.LED CL-165HR/YG	T	102.8/12.4
MC1	7700002750	MIC EM9745P-38-G <HOR>		
S1	2260002840	SW SKHLLFA010		
S2	2260002800	S.SW SW-167 (SKQTLAE010)	B	99.4/44.2
S3	2260002800	S.SW SW-167 (SKQTLAE010)	B	60.9/44.2
S4	2250000490	ECR TP70TF5163-15.9F-2775		
EP1	6910015370	S.BEA ACZ1005Y-102-T	T	57/29.9
EP3	6910015370	S.BEA ACZ1005Y-102-T	T	35/32

[ANT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
L601	6200008240	S.COL 0.30-0.9-5TL 14N	B	7.2/12.5
C601	4030017600	S.CER ECJ0EC1H080C	B	5.8/15.3

[CONNECT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C501	4030017460	S.CER ECJ0EB1E102K	T	8.3/5.3
C502	4030016930	S.CER ECJ0EB1A104K	T	9.3/5.3
J501	6910016390	CNR IMSA-9230B-1-02Z145-PT1		

• BC-160

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
IC1	1110006480	S.IC NJM2801U1-0543-TE1	B	10.2/62.3
IC2	1110003071	S.IC μPC494GS-E1-A	B	13/36.7
IC3	1140012301	S.IC μPD789112AMC-534-5A4-A	B	19.1/19.6
IC4	1110002700	S.IC NJM2904M-TE1	B	35.1/13.8
Q1	1530002060	S.TR 2SC4081 T106 R	B	37.3/63.9
Q2	1550000090	S.FET RSQ035P03TR	B	37.3/60.9
Q3	1530002060	S.TR 2SC4081 T106 R	B	35.8/19.3
Q4	1530002060	S.TR 2SC4081 T106 R	B	41.6/18.3
Q5	1590000430	S.TR DTC144EUA T106	B	23.7/26.6
Q6	1530002060	S.TR 2SC4081 T106 R	B	22.5/58.2
D1	1730002350	S.ZEN MA8110-M (TX)	B	17.6/60.5
D2	1750000550	S.DIO 1SS355 TE-17	B	34.8/64.4
D3	1750001110	S.DIO SM240A-T	B	44.4/56
D4	1160000070	S.DIO DAN202K T146	B	26.9/20.6
D5	1750000550	S.DIO 1SS355 TE-17	B	27.2/15
X1	6060000790	S.CER CSTCR4M91G	B	10.3/17.7
L1	6190001640	S.COL SLF12555T-101M1R1	B	35.3/52.7
L2	6200002611	S.COL NLV25T-R47J	B	20.8/28.2
R2	7030000460	S.RES MCR10EZJH 4.7 k	B	20.3/58.6
R3	7030003410	S.RES ERJ3GEYJ 561 V (560)	B	37.3/65.8
R4	7030003200	S.RES ERJ3GEYJ 100 V (10)	B	34.6/61.1
R5	7030009580	S.RES ERJ8RSJ R12V	B	31.8/73
R6	7030000540	S.RES MCR10EZJH 22 k	B	30.1/26.8
R7	7030000380	S.RES MCR10EZJH 1 k	B	30.1/29.6
R8	7030003520	S.RES ERJ3GEYJ 472 V (4.7 k)	B	39.5/18.4
R9	7030003600	S.RES ERJ3GEYJ 223 V (22 k)	B	13.8/30.5
R10	7030000740	S.RES MCR10EZJH 1 M	B	25.8/34.9
R11	7030000540	S.RES MCR10EZJH 22 k	B	24.8/37.8
R12	7030003560	S.RES ERJ3GEYJ 103 V (10 k)	B	10.8/30.5
R13	7030003600	S.RES ERJ3GEYJ 223 V (22 k)	B	19.3/34.5
R14	7030003770	S.RES ERJ3GEYJ 564 V (560 k)	B	21/34.5
R15	7030003650	S.RES ERJ3GEYJ 563 V (56 k)	B	21/40.3
R16	7030003770	S.RES ERJ3GEYJ 564 V (560 k)	B	19.3/40.3
R17	7030003560	S.RES ERJ3GEYJ 103 V (10 k)	B	22.7/40.3
R18	7030003410	S.RES ERJ3GEYJ 561 V (560)	B	8.6/43.5
R19	7030003620	S.RES ERJ3GEYJ 333 V (33 k)	B	16.7/42.1
R20	7030000560	S.RES MCR10EZJH 33 k	B	28.1/40.4
R21	7030000380	S.RES MCR10EZJH 1 k	B	26.3/28.6
R22	7030000440	S.RES MCR10EZJH 3.3 k	B	24/11.4
R23	7030000460	S.RES MCR10EZJH 4.7 k	B	24/8.8
R24	7030000260	S.RES MCR10EZJH 100 (101)	B	20.3/11.4
R25	7030000260	S.RES MCR10EZJH 100 (101)	B	20.3/8.8
R26	7030000500	S.RES MCR10EZJH 10 k	B	30.5/22
R27	7030007220	S.RES ERA3YED 202V (2 k)	B	30.2/19.6
R28	7030011200	S.RES ERA3YEB 303V (30 k)	B	30/18.1
R29	7030011190	S.RES ERA3YEB 103V (10 k)	B	26.9/16.6
R30	7030005871	S.RES ERA3YKD 104V (100 k)	B	40.4/15.1
R31	7030003560	S.RES ERJ3GEYJ 103 V (10 k)	B	29.8/15.9
R32	7030005341	S.RES ERA3YED 332V (3.3 k)	B	43.4/11.1
R33	7030000500	S.RES MCR10EZJH 10 k	B	31.7/9.8
R34	7030000740	S.RES MCR10EZJH 1 M	B	42.1/14.4
R35	7030003440	S.RES ERJ3GEYJ 102 V (1 k)	B	40.4/12.2
R36	7030000460	S.RES MCR10EZJH 4.7 k	B	34.7/23.8
R37	7030005501	S.RES ERA3YKD 124V (120 k)	B	33.6/21.3
R38	7030005671	S.RES ERA3YKD 393V (39 k)	B	30.1/25.1
R39	7030000010	S.RES MCR10EZJH JPW	B	28.1/42.2
R40	7030000010	S.RES MCR10EZJH JPW	B	27.7/8.4
R41	7030000010	S.RES MCR10EZJH JPW	B	34.6/9.2
R42	7030008240	S.RES ERJ12YJ0R00U	B	38.9/7.4
R43	7030000010	S.RES MCR10EZJH JPW	B	30.1/33.3
R44	7030000010	S.RES MCR10EZJH JPW	B	28.1/33.3
R45	7030000010	S.RES MCR10EZJH JPW	B	29.1/38
R46	7030000010	S.RES MCR10EZJH JPW	B	29.1/36.1
R47	7030000010	S.RES MCR10EZJH JPW	B	43.9/18.3
R48	7030008240	S.RES ERJ12YJ0R00U	B	43/28.9
R49	7030000010	S.RES MCR10EZJH JPW	B	23.5/5.7
R50	7030008240	S.RES ERJ12YJ0R00U	B	34.1/38.2
R51	7030000010	S.RES MCR10EZJH JPW	B	23.9/34.9
R52	7030000010	S.RES MCR10EZJH JPW	B	24.7/32
R53	7030008240	S.RES ERJ12YJ0R00U	B	38.6/33.1
R54	7030000010	S.RES MCR10EZJH JPW	B	34.4/33
R55	7030000010	S.RES MCR10EZJH JPW	B	32/60.1
R56	7030000010	S.RES MCR10EZJH JPW	B	42.1/41.5
R57	7030000010	S.RES MCR10EZJH JPW	B	37.2/41.5
R58	7030000010	S.RES MCR10EZJH JPW	B	24.9/57
R59	7030000010	S.RES MCR10EZJH JPW	B	27.6/49.3
R60	7030000010	S.RES MCR10EZJH JPW	B	16.3/58.3
R61	7030000010	S.RES MCR10EZJH JPW	B	4.9/31.7
R62	7030000010	S.RES MCR10EZJH JPW	B	39.1/41.5
R63	7030000010	S.RES MCR10EZJH JPW	B	31.4/43.6
R64	7030000010	S.RES MCR10EZJH JPW	B	40.1/38.7
R65	7030000010	S.RES MCR10EZJH JPW	B	4.9/49.5
R66	7030003560	S.RES ERJ3GEYJ 103 V (10 k)	B	8.2/13.6
R67	7030000100	S.RES MCR10EZJH 4R7 (4.7)	B	10.2/45.1
C1	4030006900	S.CER C1608 JB 1H 103K-T	B	44.5/70.7
C2	4030006900	S.CER C1608 JB 1H 103K-T	B	48.2/73.5

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)
S.=Surface mount

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C3	4030006860	S.CER C1608 JB 1H 102K-T	B	44.5/67.8
C4	4030006900	S.CER C1608 JB 1H 103K-T	B	32.9/69.7
C5	4030006900	S.CER C1608 JB 1H 103K-T	B	32.9/71.1
C6	4510008540	S.ELE EEE1CA100SR	B	17.5/63.8
C7	4030011600	S.CER C1608 JB 1E 104K-T	B	13.4/60.8
C8	4030006900	S.CER C1608 JB 1H 103K-T	B	9.2/58.7
C9	4030011600	S.CER C1608 JB 1E 104K-T	B	13.4/63.8
C10	4510009150	S.ELE EEE1EA470WP	B	43.6/62.8
C11	4030006900	S.CER C1608 JB 1H 103K-T	B	35.8/67.9
C12	4030006900	S.CER C1608 JB 1H 103K-T	B	32.4/67.9
C13	4510009150	S.ELE EEE1EA470WP	B	26.5/62.8
C14	4510008660	S.ELE EEE0JA220SR	B	34.3/28
C15	4510008660	S.ELE EEE0JA220SR	B	40.8/23.8
C16	4030006860	S.CER C1608 JB 1H 102K-T	B	12.3/30.5
C17	4030011600	S.CER C1608 JB 1E 104K-T	B	19.3/37.4
C18	4030006900	S.CER C1608 JB 1H 103K-T	B	21/37.4
C19	4030006900	S.CER C1608 JB 1H 103K-T	B	13.1/42.2
C20	4030009980	S.CER C1608 JB 1H 152K-T	B	8.6/42.1
C21	4030011600	S.CER C1608 JB 1E 104K-T	B	9.5/21.9
C22	4030006900	S.CER C1608 JB 1H 103K-T	B	19/25.5
C23	4030006900	S.CER C1608 JB 1H 103K-T	B	26.9/23.2
C24	4030006900	S.CER C1608 JB 1H 103K-T	B	26.9/18
C25	4030004760	S.CER C2012 JF 1H 104Z-T	B	33.2/17.5
C26	4030006900	S.CER C1608 JB 1H 103K-T	B	41.9/11.1
C27	4030006900	S.CER C1608 JB 1H 103K-T	B	29.5/12.6
C28	4030006900	S.CER C1608 JB 1H 103K-T	B	30.1/23.7
J1	6510024940	CNR HEC2305-016250		
DS1	5040002740	LED RT3-03HRYG		

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)
S.=Surface mount

SECTION 8

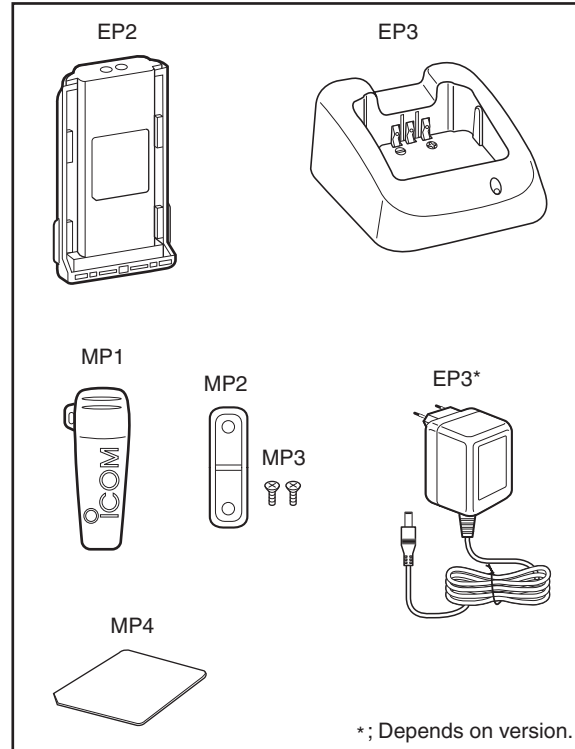
MECHANICAL PARTS

[CHASSIS PARTS]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
J2	6910015860	IMSA-6277S-O2A-G	1
SP1	2510001061	K036NA500-67	1
W1	8900009640	OPC-963	1
EP1	3310003640	2927 ANT	1
MP1	8010019694	2775 CHASSIS-4	1
MP2	8210020920	2775 FRONT PANEL (Incl. MP3, MP4, MP5, MP6, MP7)	1
MP3	8210020820	2775 PTT PANEL	1
MP4	8930063360	2775 PTT BUTTON	1
MP5	8930063370	2775 PTT RUBBER	1
MP6	8930040390	Speaker net (B)	1
MP7	8930046050	Speaker net (C)	1
MP8	8210020550	2721 REAR PANEL	1
MP9	8930063350	2775 LENS	1
MP10	8610011930	KNOB N-318	1
MP11	8610012130	KNOB N-323	1
MP13	8930063330	2775 B-MAIN SEAL	1
MP14	8930063060	2721 T-RUBBER	1
MP16	8930063400	2775 SIDE PLATE	1
MP17	8930063410	2775 B-TOP PLATE	1
MP20	8930043760	1923 MIC SEAL	1
MP21	8930059360	2600 RELEASE BUTTON	1
MP22	8930070361	2775 RELEASE PLATE (A)-1	1
MP23	8610007510	knob spring NO.7800	1
MP24	8610007920	knob spring NO.1500	1
MP25	8830002900	2927 ANT NUT	1
MP26	8810009221	Screw BT B0 2X8 NI-ZK3 (BT)	2
MP27	8810009561	Screw BT B0 2X6 NI-ZK3 (BT)	2
MP28	8810009511	Screw BT B0 2X4 NI-ZC3 (BT)	9
MP29	8810009511	Screw BT B0 2X4 NI-ZC3 (BT)	1
MP30	8810009511	Screw BT B0 2X4 NI-ZC3 (BT)	1
MP31	8810010430	screw truss M3X5 SUS SSBC	1
MP32	8930051290	2251 OPT SHEET	1
MP33	8930042350	1922 MIC SHEET	1
MP34	8930056540	Push spring (AH)	2
MP35	8830001701	VR NUT (Q)-1	1
MP36	8830001701	VR NUT (Q)-1	1
MP38	6910018220	2927 ANT CAP	1

[ACCESSORIES]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
EP2	Optional product	BP-232N [EUR-17], [UK-17]	1
	Optional product	BP-230N [EUR-18], [UK-18]	1
EP3	Optional product	BC-160 [EUR-17], [UK-17]	1
	Optional product	BC-171 [EUR-18], [UK-18]	1
EP4	Optional product	BC-145E [EUR-17]	1
	Optional product	BC-145UK [UK-17]	1
	Optional product	BC-147E [EUR-18]	1
MP1	Optional product	MB-94	1
MP2	8210020560	2721 JACK PANEL	1
MP3	8810004861	Screw PH M2X6 ZK3	2
MP4	8930051290	2251 OPTION SHEET	1



[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
J2	6450001680	HSJ1122-010010	1
J3	6450002250	HSJ1456-010320	1
MC1	7700002750	EM9745P-38-G	1
S1	2260002840	SKHLLFA010	1
S4	2250000490	TP70TF5163 15.9F-2775	1
MP1*	8410002530	2681 PA HEATSINK	1
MP2	8510016460	2775 VCO COVER	1
MP3*	8510016470	2775 VCO CASE	1
MP4*	8510016580	2775 SHIELD PLATE	1
MP5	8510016770	2776 EARTH PLATE	1

*: Refer to SECTION 10 BOARD LAYOUTS.

[ANT UNIT]

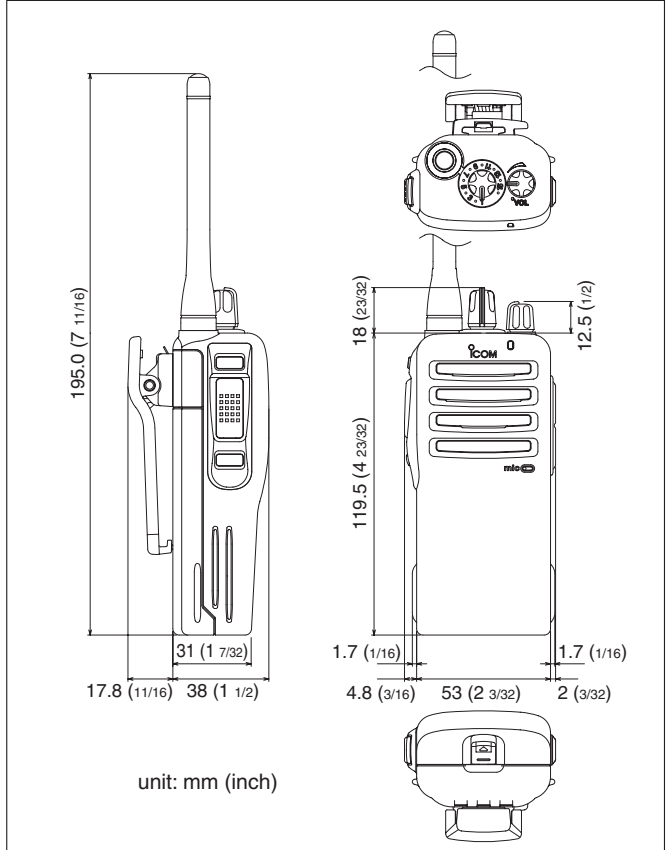
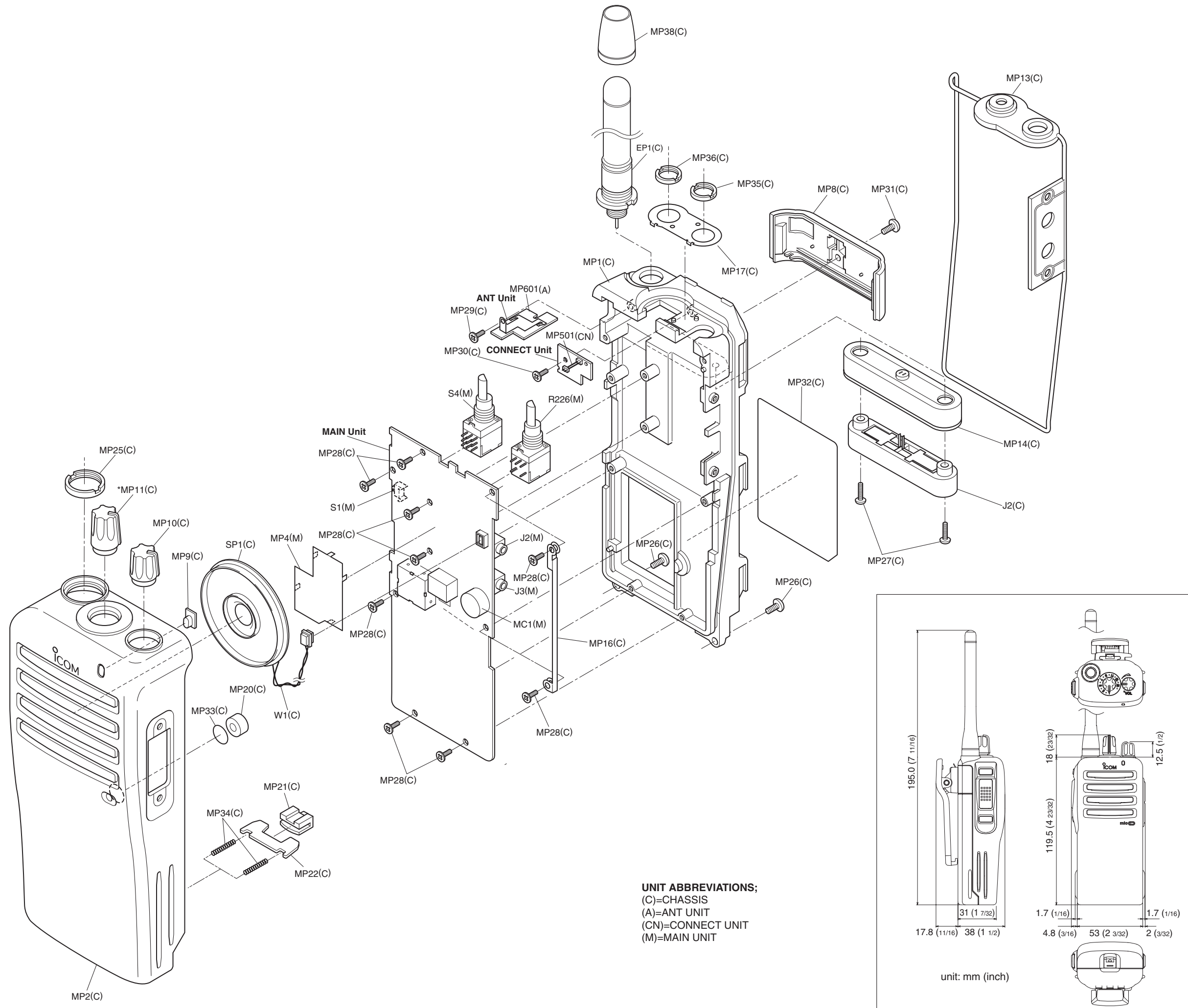
REF NO.	ORDER NO.	DESCRIPTION	QTY.
MP601	8510016350	2721 ANT PLATE	1

[CONNECT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
J501	6910016390	IMSA-9230B-1-02Z145-PT1	1

Screw abbreviations

A, B0, BT: Self-tapping PH: Pan head ZK: Black NI-ZU: Nickel-Zinc SUS: Stainless



SECTION 9 SEMICONDUCTOR INFORMATION

• TRANSISTERS AND FETs

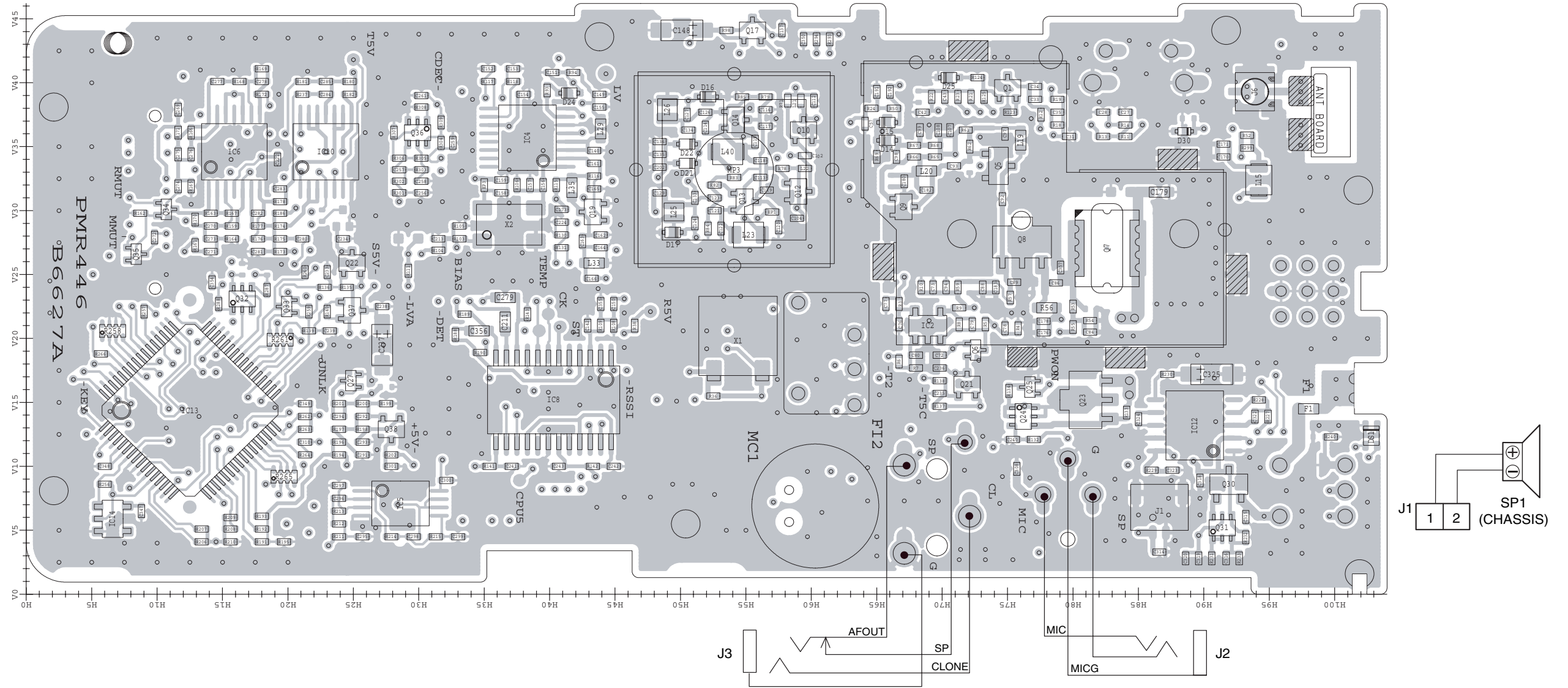
NAME	SYMBOL	INSIDE VIEW
2SA1577 R	HR	
2SB1132 R	BARB	
2SC3356 R25 2SC4116 BL 2SC4215 O 2SC4226 R25 2SC5006 2SC5700	R25 LL QO R25 24 WB	
2SK1829 F	KI	
2SK3019	KN	
2SK880 Y F	XY	
3SK293 F 3SK324	UF UG	

NAME	SYMBOL	INSIDE VIEW
DTA114EU UNR9111J UNR9113J	16 6A 6C	
RD01MUS1	K2	
RD07MVS1	RD07MVS1	
UNR9213J	8C	
XP1214	9H	
XP4601	5C	
XP6501 AB	5N	

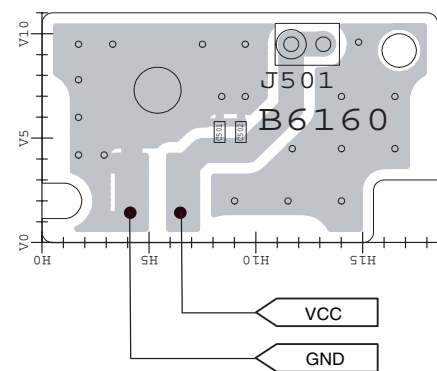
• DIODES

NAME	SYMBOL	INSIDE VIEW
1SV307	TX	
DAN222	N	
HVC350B-E	B0	
MA2S077 MA2S111 MA2S728	S A B	
MA368	6L	
RB706F-40	3J	

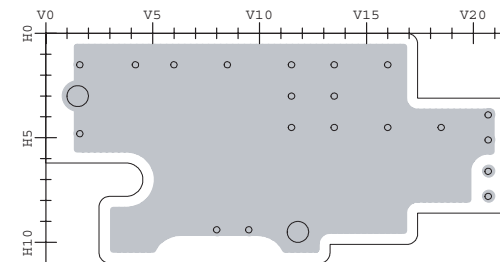
• MAIN UNIT (TOP VIEW)



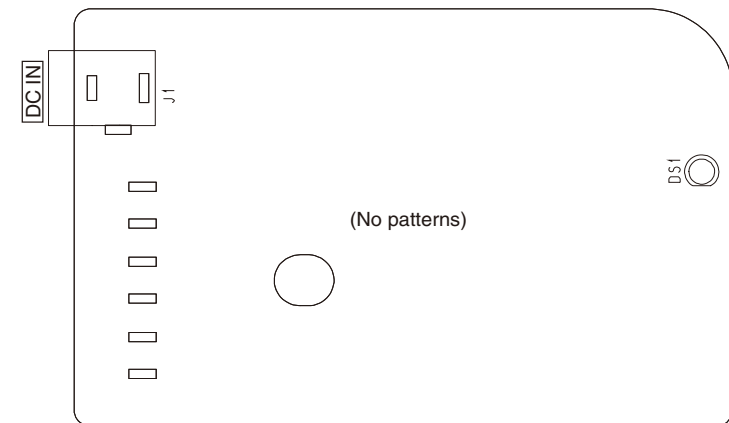
• CONNECT UNIT (TOP VIEW)



• ANT UNIT (TOP VIEW)

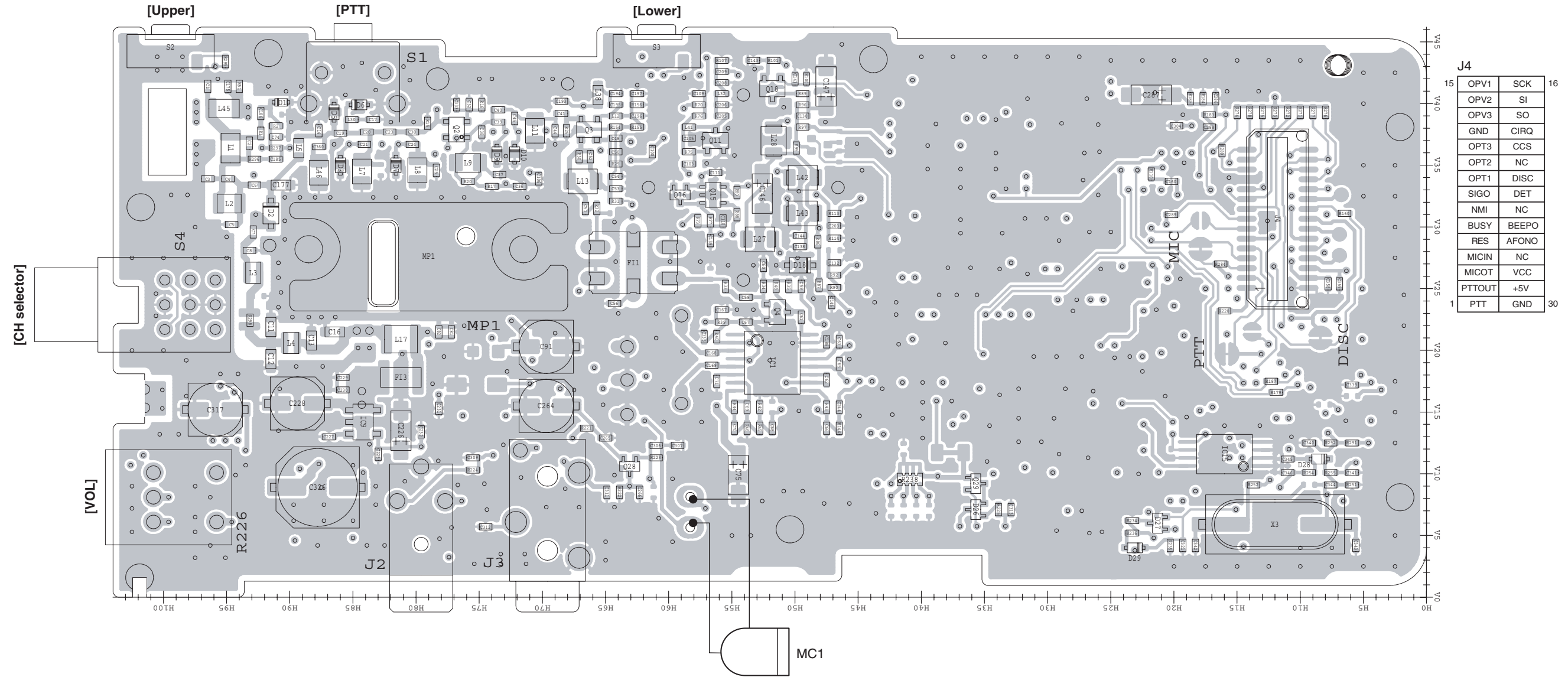


• BC-160 (TOP VIEW)

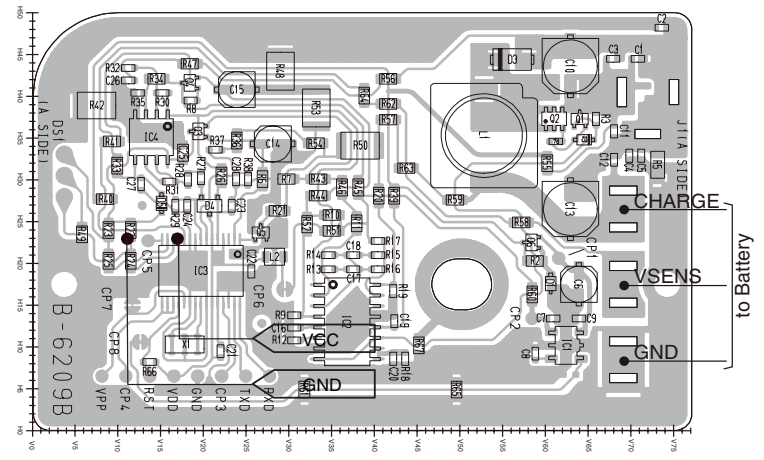


The combination of this side and the bottom side shows the board layout in the same configuration as the actual P.C.Board.

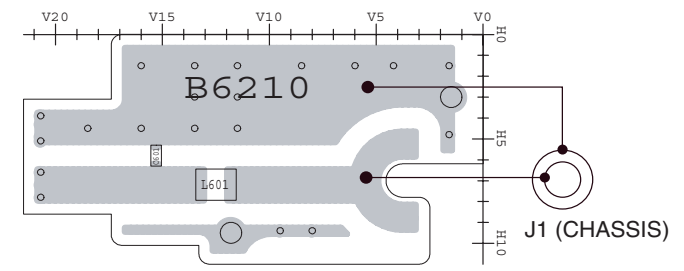
• MAIN UNIT (BOTTOM VIEW)



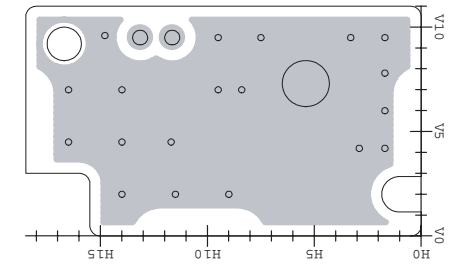
• BC-160 (BOTTOM VIEW)

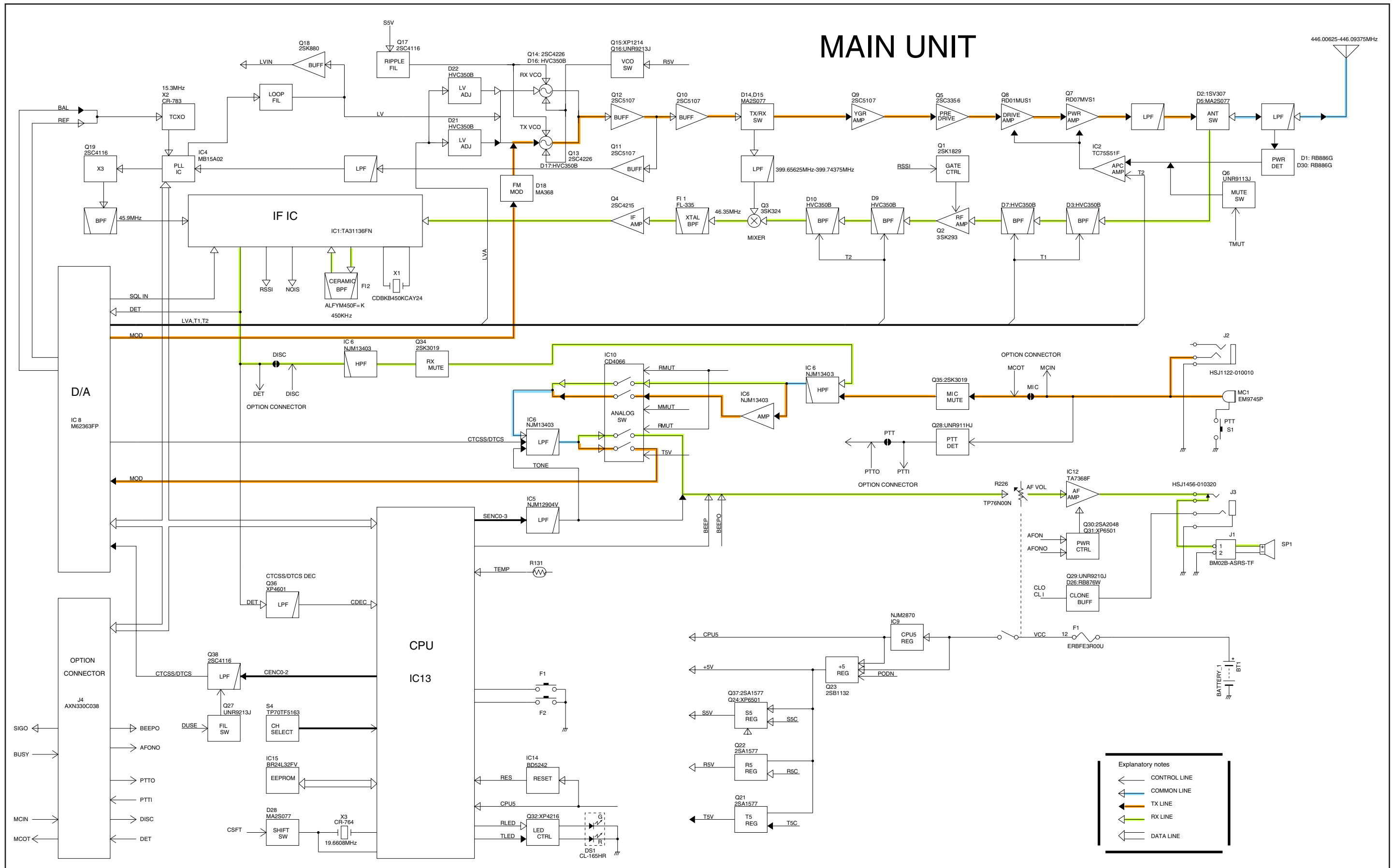


• ANT UNIT (BOTTOM VIEW)



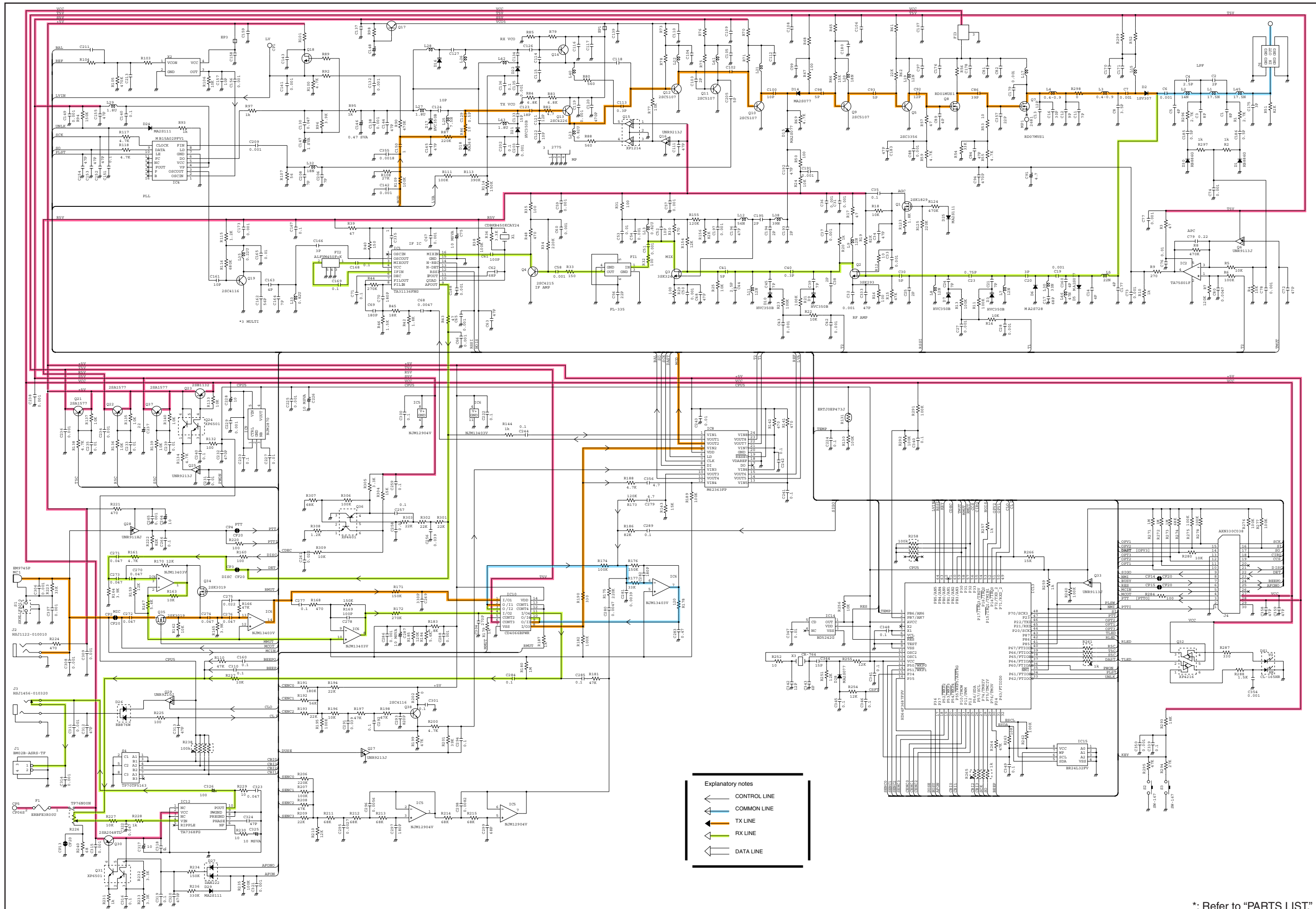
• CONNECT UNIT (BOTTOM VIEW)





SECTION 12

VOLTAGE DIAGRAM



*: Refer to "PARTS LIST."

SECTION 13

BC-160

[CHASSIS PARTS]

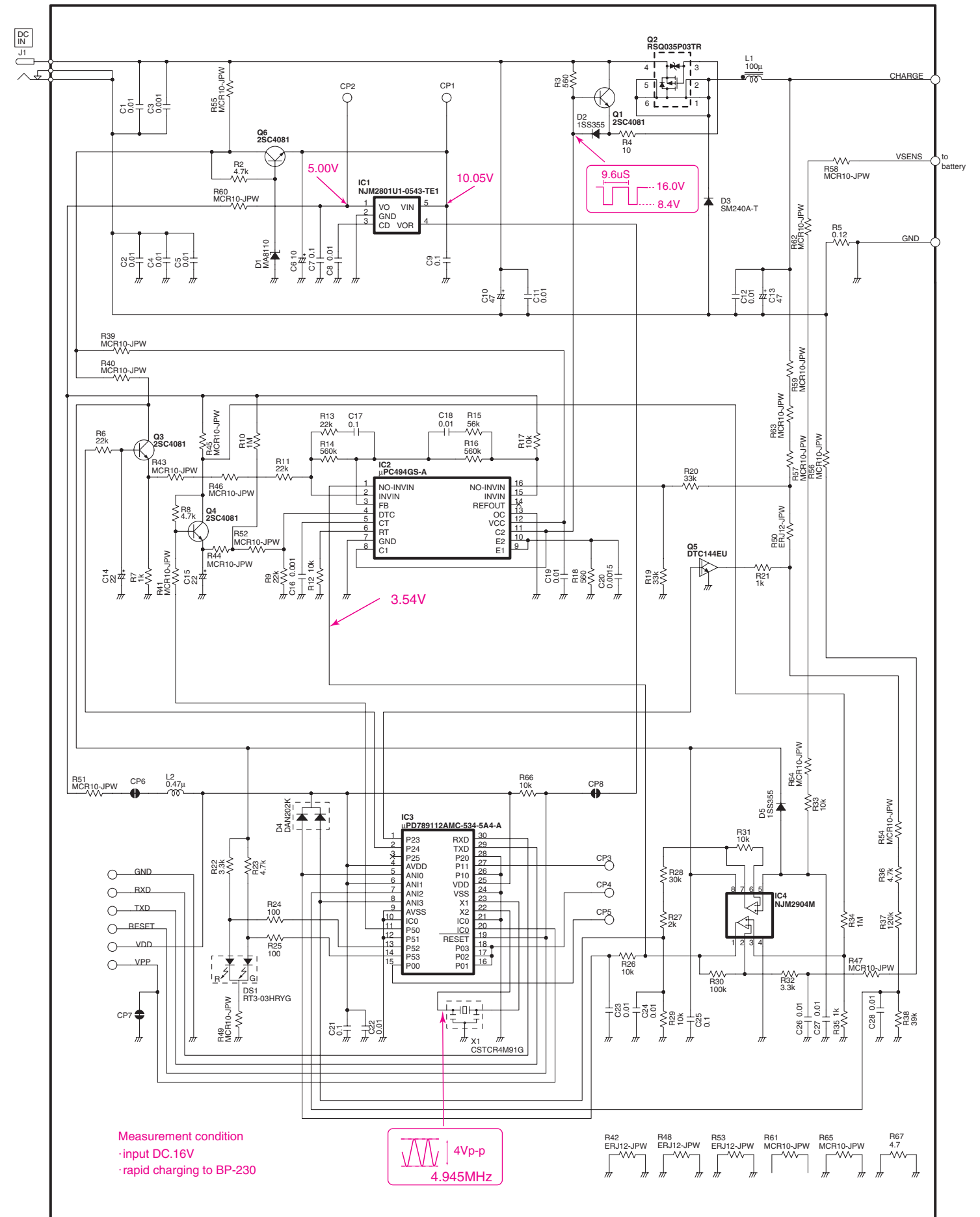
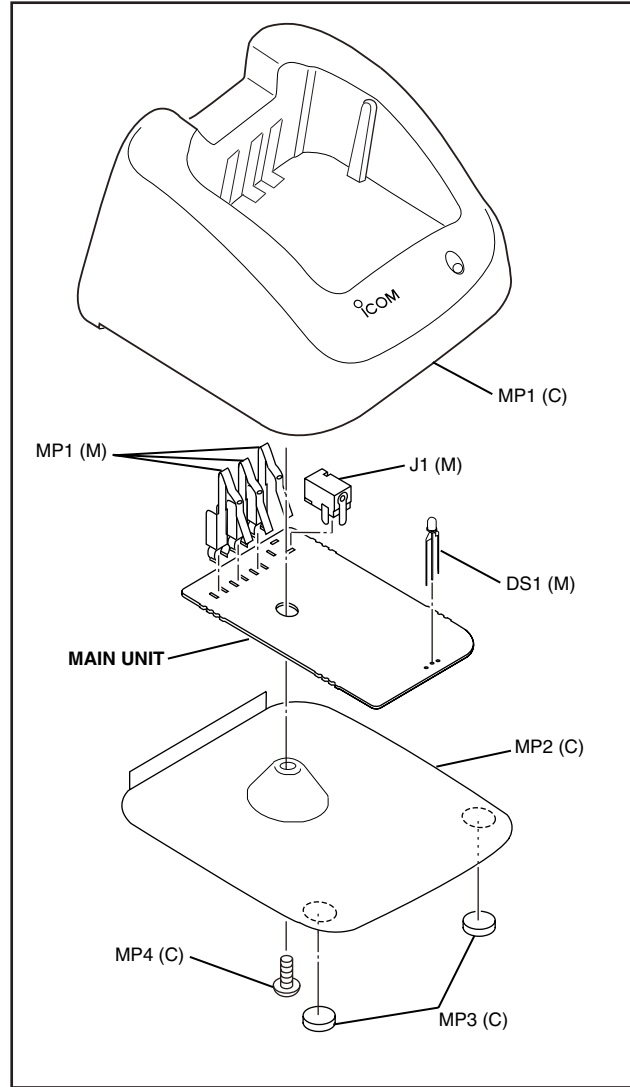
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
MP1	8010019750	2830 case	1
MP2	8110008220	2830 cover	1
MP3	8930039620	Leg cushion (A)	2
MP4	8810008630	Screw PH BT M3 x 6 NI-ZU	1

[MAIN UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6510023070	Connector HEC2305-01-250	1
DS1	5040002740	LED RT3-03HRYG	1
MP1	8930064410	2830 TERMINAL	3

[ACCESSORIES]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
EP1	Optional product	Charger BC-145E	[EUR] 1
	Optional product	Charger BC-145UK	[UK] 1



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